LISTING OF THE CLAIMS

This Listing of Claims will replace all prior versions and listings of claims in this application.

Listing of Claims:

1. (Currently amended) A system for accessing a two way associative cache having first and second ways, comprising:

a clock circuit for selectively applying clock pulses to one or to both ways of said two way associative cache in response to an access mode signal, a HITA signal and a HITB signal;

an effective address register connected to simultaneously apply an address to each of said two way associative cache;

an output multiplexer for selecting data from one of said first and second ways of said two way associative cache in response to a select signal identifying one of said ways of said associative cache; and

a byte select circuit configured to select an individual byte of the data selected by the output multiplexer in accordance with byte data contained in the effective address register,

wherein, in a power efficiency access mode, the clock circuit is configured such that the access mode signal enables the HITA signal and the HITB signal to select~~said select signal selects~~ one of said first way and second way to apply clock pulses to at an end of an access cycle, and

wherein, in a high speed access mode, the clock circuit is configured such that the access mode signal disables the HITA signal and the HITB from selecting and both of said first way and second way have clock pulses applied.

2. (Previously presented) A system for accessing a two way associative data cache according to claim 1 further comprising:

a tag array connected to be addressed by said address circuit for storing first and second sets of tag signals corresponding to a corresponding set of data stored in said first and second ways; and

first and second comparators connected to compare first and second output data from said tag array with tag data derived from said address,

thereby identifying one of said ways of said associative caches containing data to be read, said one comparator generating the select signal for said output multiplexer.

3. (Previously presented) The system according to claim 1 wherein said access mode signal applies clock pulses to both ways of said associate cache when the access time for reading said data from one of said sets is less than a predetermined amount.

4. (Previously presented) The system according to claim 1 wherein said access mode signal is generated from prediction logic which predicts which of said first and second ways of said two way associative cache contains said data.

5. (Original) The system according to claim 2 wherein said clock circuit receives data from said comparator identifying which of said ways of said associative cache is to be clocked.

6. (Previously presented) The system according to claim 5 wherein in a high speed access mode, said clock circuit receives an access mode signal which indicates that both of said sets of associative cache are to be clocked simultaneously.

7. (Previously presented) The system according to claim 6 wherein said access mode signal is selected based upon a need to conserve power by only applying clock pulses to one way of said data cache, or to provide higher access speed to said data cache by applying clock pulses to both ways of said data cache.

8. (Currently amended) A system for accessing a data cache having at least two ways for storing data at the same addresses, comprising:

a first and second tag memory for storing first and second sets of tags identifying data stored in each of said ways;

a translation device for determining from a system address a tag identifying one of said ways;

a first comparator for comparing tags in said address with a tag stored in said first tag memory;

a second comparator for comparing a tag in said address with a tag stored in said second tag memory;

a multiplexer for selecting output data from one of said ways in response to a select signal from one of said first and second comparators;

a byte select circuit configured to select an individual byte of the data selected by the output multiplexer in accordance with byte data contained in the effective address register; and

a clock signal circuit for supplying clock signals to one or both of said ways in response to an access mode signal, a HITA signal and a HITB signal,

wherein, in a power efficiency access mode, the clock circuit is configured such that the access mode signal enables the HITA signal and the HITB signal to selectsaid select signal selects one of said first way and second way to apply clock pulses to at an end of an access cycle, and

wherein, in a high speed access mode, the clock circuit is configured such that the access mode signal disables the HITA signal and the HITB from selecting and both of said first way and second way have clock pulses applied.

9. (Previously presented) The system according to claim 8 wherein said access mode signal has a first state which represents the power efficiency access mode of operation.

10. (Previously presented) The system according to claim 9 wherein said access mode signal has a second state which represents a high speed access mode for said cache.

11. (Previously presented) The system according to claim 9 wherein said access mode signal is in said first state when said access speed is one half of a maximum access speed for said cache.

12. (Currently amended) A method for accessing a set associative data cache comprising at least two ways, comprising:

determining from an effective address tag associated with data stored in one of said ways;

addressing said first and second ways with identical Line Index addresses derived from said effective address;

addressing first and second tag memories with said Line Index address applied to said first and second ways;

determining whether said first or second tag memories produce a tag identical to said tag determined from said effective addresses;

supplying clock signals to one or both of said ways in response to an access mode signal, a HITA signal and a HITB signal;

selecting an individual byte of data selected by an output multiplexer in accordance with byte data contained in an effective address register; and

reading data from one of said ways in response to a first state of an access mode signal, and reading data from both of said ways when said access mode signal has a second state,

wherein, in a power efficiency access mode, the clock circuit is configured such that the access mode signal enables the HITA signal and the HITB signal to selectsaid select signal selects one of said first way and second way to apply clock pulses to at an end of an access cycle, and

wherein, in a high speed access mode, the clock circuit is configured such that the access mode signal disables the HITA signal and the HITB from selecting and both of said first way and second way have clock pulses applied.

13. (Previously presented) The method for accessing a set associative data cache according to claim 12 wherein said first state of said access mode signal is selected when said data cache is read in a power conserving mode, and said second state of said access signal is selected when said data cache is operated in a high speed access mode.

14. (Original) The method for accessing a set associative data cache according to claim 12 wherein said access mode signal controls a clock circuit that applies a clocking signal to said first way in said first state, and applies clocking signals to both ways when said access mode signal is in said second state.

15. (Currently amended) A system for accessing a data cache having at least two ways for storing data at the same addresses, comprising:

a first and second tag memory for storing first and second sets of tags identifying data stored in each of said ways;

a translation device for determining from a system address a tag identifying one of said ways;

a first comparator for comparing tags in said address with a tag stored in said first tag memory;

a second comparator for comparing a tag in said address with a tag stored in said second tag memory;

a multiplexer for selecting output data from one of said ways in response to a select signal from one of said first and second comparators; and

a clock signal circuit for supplying clock signals to one or both of said ways in response to an access mode signal, a HITA signal and a HITB signal,

wherein said access mode signal has a first state which represents a power efficiency access mode of operation and said access mode signal is in said first state when said access speed is one half of a maximum access speed for said cache, and

wherein, in a power efficiency access mode, the clock circuit is configured such that the access mode signal enables the HITA signal and the HITB signal to select~~said select signal selects~~ one of said first way and second way to apply clock pulses to at an end of an access cycle, and

wherein, in a high speed access mode, the clock circuit is configured such that the access mode signal disables the HITA signal and the HITB from selecting and both of said first way and second way have clock pulses applied.

16. (Previously presented) The system according to claim 15 wherein said access mode signal has a second state which represents a high access speed for said cache.